JORWAY CORPORATION

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The programming and use of the Model 221A Timing and Sequence Module

INTRODUCTION

The Model 221A Timing and Sequence Module is a general purpose device, designed to provide a serial sequence of 16 time related signals. It is useful as a multi-channel programmable pulse generator or as a clock source for transient recorders. An analog output option enables a single analog waveform to be generated simultaneously with the digital waveform channels. The Model 221A, an upgrade of the popular Model 221 preserves most of the features of the Model 221 while enhancing performance and adding new features. A stored program of up to 512K set points (expanded from the former models 4K memory) determine timing and logic state of the expanded 16 output channels. Among the uses of this larger memory is the programming of a variable clock for use in clocking transient recorders.

For more specific information on the features, CAMAC commands and model differences see the Model 221A data sheet.

A 34 pin rear connector accommodates the extra 4 bits however the lower 26 pins are identical to the Model 221 for compatibility. A 26 wire ribbon cable crimped into a 34 pin header will allow connection to existing Model 221 applications.

BASIC OPERATION

The Model 221A contains two 512K memories which share a common memory address counter. The set point memory is 24 bits wide and when programmed should contain ascending numbers which represent times from the initial start of the sequence. At a system clock rate of 1 MHz the time resolution is 1 microsecond and the maximum duration for a sequence is 16.777215 seconds. At a system clock rate of 10 MHz the resolution is 0.1 microseconds and the maximum duration is 1.6777215 seconds. After a start, the contents of the first setpoint memory location are compared to a 24 bit address counter which counts the system clock beginning at the start time. At coincidence the contents of the 16 bit wide memory are latched into an output register which determines the state of the modules 16 channel outputs until the next set point. At each ascending setpoint coincidence the output latches are updated with the output memory contents for that memory address. Once the module is started, all other start trigger inputs are ignored until either a stop, reset and disable operation occur. Once triggered and cycle active, the application of a stop trigger will cause the cycle to be put on hold. At this point operation will not continue and the sixteen outputs will remain in their current state. The subsequent application of a start trigger input will cause the cycle to continue from the point where "hold" occurred.

For fewer than the maximum number of set points, all ones (16,777,215) written into the set point memory will terminate cycle execution. Cycle execution is also terminated by:

(a) address overflow (greater than 512K set points). The 24 bit address counter accommodates up to 16,777, 214 possible set point addresses. Only a maximum of 512K (524,288) discrete addresses are available.

(b) Set point overflow (compare counter overflow). Occurs when the compare counter reaches 16,777,215 while searching for a comparison with the set point number. This will occur if the set point memory encounters an address which is smaller than the previous address (i.e. not ascending).

(c) any command which terminates the active cycle (F(9)·A(0) or ZS2.

Memories can be written as well as read from the dataway to aid in diagnostic testing. A common 24 bit address counter is used for both memories which is auto incremented for read or write. A separate load memory address counter command allows access to single memory words for read or write.

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MODULE PROGRAMMING

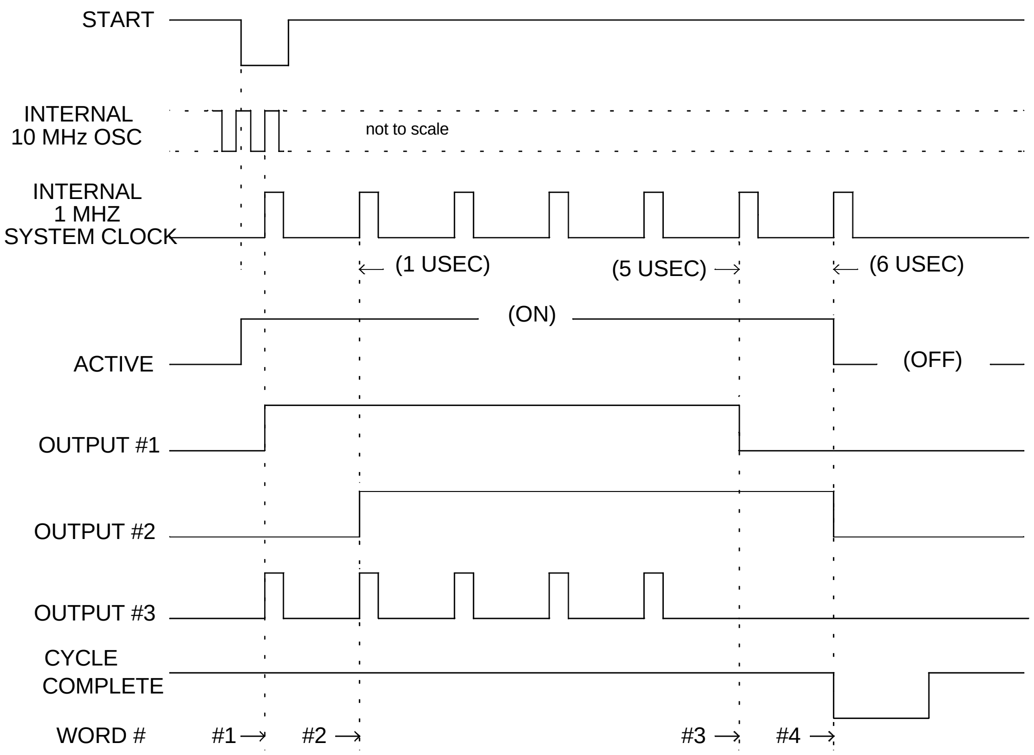
A Simple Example (Internal Oscillator, 1 MHz system clock selected)

The following example is provided to illustrate a simple programmed sequence. The module is initially reset assuring that the active state is disabled. This reset by either Z·S2 or F(9)·A(0) will also clear the memory address to zero. Otherwise a write memory address F(16)·A(2) with 0 data may be used. The set point memory must be loaded with ascending values starting from the value used at start which could be address zero. If a mistake is made and set points are not ascending, once started the comparitor will search until a address counter overflow occurs which will take 16.7 seconds. During this time the ACT LED (active) will remain on. Following the set to address zero the memories can now be loaded. The following is an illustration of a memory load sequence which is given after the memory address has been set to zero:

STEP #	COMMAND	DATA VALUE	STEP #	COMMAND	DATA VALUE
1	F(16)·A(0)	Data=5, Word 1	6	F(16)·A(1)	Data=0 (Word 1 occurs at start time)
2	F(16)·A(0)	Data=7, Word 2	7	F(16)·A(1)	Data=1 (Word 2 occurs at 1 usec)
3	F(16)·A(0)	Data=2, Word 3	8	F(16)·A(1)	Data=5 (Word 3 occurs at 5 usec)
4	F(16)·A(0)	Data=0, Word 4	9	F(16)·A(1)	Data 16,777,215 (Word 4 indicates sequence is to be terminated).
5	F(9)·A(0)	(Clear address to zero)	10	F(9)·A(0)	(Clear address to zero)

After the load operation, the memory can be read back if desired but a clear memory address must be the last command to assure address 0. This sample program includes output channel #3 programmed for the Gated Clock Option. This is accomplished by a F(18)·A(1) with data = 4. This sets the Gated Clock register with a "1" at bit 3 for channel 3 resulting in the output of the 1 MHz System Clock during word 1 and word 2.

An output cycle sequence is executed by F(26)·A(1) to enable Output Word then either F(25)·A(0) for dataway start or F(26)·A(2) and External Start. The following output will occur:



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To repeat the sequence an enable output F(26)·A(1) and an appropriate start may be required. In this illustration the Cycle Complete Output is inverted i.e. the program switch #6 is set to OFF or (-) for Cycle Complete. If switch # 9 were to be set OFF (Recycle Enabled) and the Cycle Complete LEMO connected to the Start LEMO Input, after a program start, the sequence would repeat until halted by the HOLD function, disable external start F(24)·A(2) or reset F(9)·A(0). A initialize Z may be used as well but External Start enable and Output enable will also have to be set again prior to the next start command. Note that the Cycle Complete pulse and the Start Input should be set so that the start occurs on the trailing edge of Cycle Complete; that is Cycle Comp at (-) and Start at (+).

Following reset, the output is normally disabled assuming Recycle is disabled. When the Output is enabled by the command F(26)·A(1) all outputs will be low because the output register has been cleared prior to a sequence start. At the end of a sequence the output will go low because of both the output disable and a reset which occur when the sequence terminates. Even during a Recycle mode as described above the Outputs will return low momentarily as the memory address counter and output register are cleared. If it is desired to have an output with an initial value high after reset the Output Polarity Option can be employed. If a “1” is written by F(18)·A(2) into the Output Polarity register, that channel will have a quiescent high level after a reset operation or whenever the output is disabled. For the channel selected for polarity reversal a programmed “1” in the Output Memory will produce a low signal for this inverted channel.

Note that in the example address zero has been used as a set point and address 0 is also an output word for channels 1 and 3. When operating with a 10 MHz system clock because of circuit delays in starting a sequence the first output edge of output 1 or 3 (Gated Clock) may be delayed by approximately 7 nanoseconds. Thereafter all edges are uniformly spaced. If this is objectionable address 0 should be avoided as a set point. At a 1 MHz system clock delays at address 0 are negligible.

CLOCK RATES AND SYNCHRONIZATION

The Model 221A can be operated from either an internal oscillator or a external clock. A user selectable program switch allow the selection of either internal or external clock as well as a number of other modes which affect both the sequence timing resolution and the CLOCK OUTPUT LEMO signal. These program switches also allow multiple modules to operate from the same clock source for better synchronizing of waveforms. A Master/Slave mode enables one master module to be used as the start and end of sequence and the slave modules to operate in unison as if they were just a wider versions of the master i.e. 32, 48 or 64 simultaneous channels

In the standard internal mode a 10 MHz crystal oscillator is counted down to 1 MHz to form a basic system clock of 1 MHz (program increments are 1 microsecond). When a sequence is started, this countdown is initiated so the first 1 usec system clock occurs within 100 to 200 nsec to reduce start jitter. When the divide by 10 clock selection is made the start jitter may be up to 2 usec for a system clock of 100 KHz (program increments are 10 usec). A new rate for the Model 221A allows the 10 MHz oscillator (Program switch #1 OFF) to be used directly as the system clock. When this 10 MHz selection is made the start jitter will be 100 nsec. The clock divide by 10 (switch #2) is not operative with this selection. Table 1 illustrates some of the various switch positions and their relationship on system clock resolution and synchronization

Operation of Multiple modules from one clock source.

When it is desired to have multiple modules operate from the same clock source a number of choices are available. Method A and B allow each module to operate with its own triggers while having the same clock source. Each module will be subject to its own start jitter and although each sequence is based on the same clock, may have its waveforms offset by the start jitter for each module. Method C provides synchronization for a Master module and Slave modules which operate from a common trigger. Start jitter applies to triggering on the master but waveforms for each module will track without any jitter between them.

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A. An External Clock can be applied to the EXT CLOCK input where 2 common connected LEMOs provide for daisy chaining of the signal to each module. In this configuration the internal 50 Ohm termination should be removed on the intermediate modules to reduce signal loading. The system clock frequency will be that of the external clock unless the internal divide by 10 is selected. In this configuration the start uncertainty or jitter will be that of one cycle of the external clock (i.e. 1 usec for a 1 MHz clock). This external clock configuration is illustrated on lines 7,8 and 9. If an external clock of 10 MHz is available and switch 2 is selected for divide by 10 the system clock will be 1 MHz as illustrated in line 10. The start jitter is also reduced to 100 nsec.

B. If one Model 221A is chosen to operate from its internal oscillator, the CLOCK OUT from that module can be used to drive the EXT CLOCK input of other connected modules so they all operate from the same oscillator. Line 1 illustrates such a module operating at a 1 MHz system clock rate while the CLOCK OUT is 10 MHz. As mentioned above the connected modules can be set to EXT CLK and divide by 10 to operate a 1 MHz as well. Jitter on the connected modules will be the 100 ns. This configuration can be operated at 10 MHz as well with the clock source module configured as in line 3 and the connected modules as in line 7.

TABLE 1
Clock Rate Selection
System Clock rates and CLOCK-OUT for various user programming switch positions.

	SW1 OFF = 10 MHz	SW2 OFF = /10	SW3 OFF = EXT CLK	SW4 OFF = M/S selected	CLK OUT Lemo	System Clock	EXT CLK Input
1.	ON	ON	ON	ON	10 MHz	1 MHz	NA
2.	ON	OFF	ON	ON	10 MHz	100 KHz	NA
3.	OFF	X	ON	ON	10 MHz	10 MHz	NA
4.	OFF	X	ON	OFF	gated 10 MHz	10 MHz	NA
5.	ON	ON	ON	OFF	gated 1 MHz	1 MHz	NA
6.	ON	OFF	ON	OFF	gated 100 KHz	100 KHz	NA
7.	ON	ON	OFF	ON	10 MHz	10 MHz	10 MHz
8.	ON	ON	OFF	ON	1 MHz	1 MHz	1 MHz
9.	ON	OFF	OFF	ON	1 MHz	100 KHz	1 MHz
10.	ON	OFF	OFF	ON	10 MHz	1 MHz	10 MHz
11.	OFF	X	OFF	ON	10 MHz	10 MHz	10 MHz
12.	OFF	X	OFF	OFF	gated 10 MHz	10 MHz	10 MHz
13.	OFF	X	OFF	OFF	gated 1 MHz	1 MHz	1 MHz
*14.	ON*	ON*	OFF*	OFF*	10 MHz	1 MHz	10 MHz
15.	ON	OFF	OFF	OFF	gated 1 MHz	1 MHz	10 MHz

Note: * This configuration with Ext. Clock is not valid for Master/Slave operations.

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C. Master/Slave Operation of multiple modules.

Multiple modules can be made to delivery their sequence from a common start and with the same system clock. This is accomplished by selecting one module as a master (SW4 OFF) which selects the CLOCK OUT LEMO of the module to output a gated system clock. This gated system clock is the clock that runs as the sequence is being generated. The Slave modules are set to be driven by the EXT CLK and are connected to the masters CLOCK OUT.

A number of steps must be taken to set up the modules for operation in this mode.

1 . All modules must have their outputs enabled by F(26)·A(1).

2. Before the sequence is to be generated all participating slave modules must be triggered for a start usually by a program start, F(25)·A(0) to each participating slave module. In a normal module this start would cause its sequence to begin, however the sequence does not begin as there is no clock present.

3. The Master module is triggered as a normal module and its sequence begins. The CLOCK OUT (gated system clock) begins and the slave modules generate their programmed sequence from this signal. At the end of each slave module sequence the output will be disabled and the address counter reset.

4. After the Master module has completed its sequence each Slave module output must be re-enabled, F(26)A(1) and triggered, F(25)A(0) to set them up for a repeat of the same operation.

In setting up the sequence programs for each module it is necessary to make sure that the master sequence length is always longer than any slave. This is required as the slaves sequence is dependent on the CLOCK OUT signal that will cease when the master sequence ends.

Use of Recycle Feature. The re-enabling of the slave modules can be eliminated in some applications by additionally enabling the Recycle setting, SW#9 on each slave module. During system initialize each slave modules Output Enable, F(26)·A(1) and External Start, F(26)·A(2) are enabled. The Cycle Complete output of the master is connected to the External Start of each slave. LEMO "T's" may have to be used and the 50 Ohm termination disabled at each intermediate slave. The master Cycle Complete polarity is set so that its trailing edge will be the slaves starts leading edge, i.e. SW#6 (-) on master and SW#7 (+) on slaves. Again under these conditions the sequence of each slave must be a shorter duration than the master to allow the Cycle Complete of the master to retrigger each slaves External Start.

Compatibility with Model 221. Most Model 221's can be used as slave modules to a Model 221A master. The Model 221 slaves are set for External Clock and a master 221A is set so gated clock do not exceed 1 MHz. The Recycle mode in Model 221's can be used as well. The only significant difference in performance is that the Model 221 output waveforms due to the slower TTL logic will be delayed approximately 400 ns from the external start signal while the Model 221A slaves are delayed only about 100 ns from the same start. In either case the jitter in the output signals is 100 ns with respect to the start but no jitter occurs with respect to the other waveforms from each module.

MODEL 221A STATUS READBACK

The Module Status register has been expanded to include status for some module switch positions, jumper positions and added features. The Model 221A has a readback of Module switch positions to aid in characterizing the module setup without taking the cover off. The positions of the 50 Ohm terminations for Lemo inputs, Inhibit Disable Jumper, and P1 & P2 Jumpers is still accessible only by cover removal. Although the 221A provides additional status information, the lower 7 bits of the status word are identical to the older Model 221 for comparability. Listed in table 2 are the significance of the Status readback word.

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TABLE 2
Module status from F(1)A(0)

	Model 221	Model 221A
Bit 1 (R1)	0 = Sequence Output Disabled, 1= enabled	same
Bit 2	0 = Sequence Output Inhibited, 1= Not Inhibited	same
Bit 3	0 = External Start Disabled, 1= Enabled	same
Bit 4	0 = Cycle Cleared, 1= Cycle Active	same
Bit 5	0 = No Cycle Hold, 1= Cycle Active but On Hold	same
Bit 6	0 = Clock divide by 1 selected 1= divide by 10	same
Bit 7	0 = Internal Clock selected 1= External Clock	same
Bit 8	Not Used	Reserved, set to 0
Bit 9	Not Used	0 = Master 1= Slave, Master/Slave Clock Switch Selection
Bit 10	Not Used	0 = positive 1 = negative, Inhibit Switch Polarity Selection
Bit 11	Not Used	0 = positive 1 = negative, Cycle Complete Switch Polarity
Bit 12	Not Used	0 = positive 1 = negative, Ext. Start Switch Polarity Selection
Bit 13	Not Used	0 = positive 1 = negative, Ext. Stop Switch Polarity Selection
Bit 14	Not Used	0 = Recycle Disabled Switch Selection 1 = Recycle Enabled
Bit 15	Not Used	0 = LAM at Cycle End Switch Selection 1 = LAM at Cycle Start
Bit 16	Not Used	Reserved, set to 0

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